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München, den 29.11.2002
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Ihr Zeichen: NC 32001 DE Ur/Wa/as

Ihr Antrag vom: 19.10.2000
auf Recherche gemäß §43 Patentgesetz

Bitte Aktenzeichen und Anmelder/Inhaber bei
allen Eingaben und Zahlungen angeben

Aktenzeichen: 100 51 889.3

Recherchebericht

A. Klassifizierung des Anmeldungsgegenstandes nach der Internationalen Patentklassifikation (IPC)

IPC 07

H 04 L 1/20

H 04 L 12/56

B. Recherchierte Gebiete

Klasse/Gruppe
H 04 L 1/20

Prüfer
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Patentabteilung
31

H 04 L 1/20 H 04 L 7/00 H 04 L 7/04 H 04 L 25/06

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C. Ergebnis der Druckschriftenermittlung

Kat.	Ermittelte Druckschriften	Erläuterungen	Betr. Ansprüche	IPC / Fundstellen
X	US 55 66 213	s. Fig. 2,5, Sp. 6, Zeile 66- Sp. 8, Zeile 40	1,11	H 04 L 7/00
X, E	WO 2001- 80 508 A	s.ges.Dok.	1-16	H 04 L 25/06

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Nachbrieftkasten
nur
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Kat.	Ermittelte Druckschriften	Erläuterungen	Betr. Ansprüche	IPC / Fundstellen
A	WO 2000- 11 831 A	s.ges.Dok.	1-16	H 04 L 7/04
X	PARK,Cheol-Hee,et.al.: Techniques for Channel Estimation,DC-Offset Compensation and Link Quality in Bluetooth System. In: IEEE,Aug.2000, Vol.46, No.3, S.682-689; s.S.684, Sp.1, Abs.1, S.685-686, Abschn.5.1 u. 5.2		1,2,11	IEEEExplore

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E. Datum des Abschlusses der Recherche 26.11.2002

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Absendedatum des Rechercheberichtes

Anlagen: 3-fach

4

Patentabteilung 1.11
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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
25 October 2001 (25.10.2001)

PCT

(10) International Publication Number
WO 01/80508 A2

(51) International Patent Classification⁷: H04L 27/00 (81) Designated States (national): CA, DE, FI, GB, JP, SE.

(21) International Application Number: PCT/US01/12638

(84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

(22) International Filing Date: 18 April 2001 (18.04.2001)

(25) Filing Language: English

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations CA, DE, FI, GB, JP, SE, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR)
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for the following designations CA, DE, FI, GB, JP, SE, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR)

(26) Publication Language: English

Published:

- without international search report and to be republished upon receipt of that report

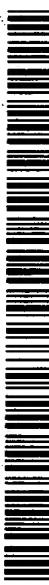
(30) Priority Data:
09/551,495 18-April 2000 (18.04.2000) US

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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(54) Title: DC OFFSET AND BIT TIMING SYSTEM AND METHOD FOR USE WITH A WIRELESS TRANSCEIVER

WO 01/80508 A2

(57) Abstract: An offset estimation and bit timing system and method. The inventive offset estimation system includes a first circuit for receiving and correlating a transmitted signal and generating a trigger signal in response thereto. A second circuit accumulates the received signal and provides a second signal on receipt of the trigger signal. The second signal is then converted to an offset error signal. In an illustrative implementation, the offset estimation system is implemented in a Bluetooth-enabled wireless receiver adapted to receive a signal transmitted with a known bit pattern. The received signal includes a plurality of messages, each message having at least one access code and each access code having a predetermined pattern therein for at least a portion thereof. The offset estimation system analyses the bit pattern and detects the DC offset in the received signal. The error signal is converted to analog and used as a reference input for the A/D converter. As an alternative, the error signal may be used to adjust the signal output by an intermediate frequency downconversion stage. The novel bit timing system includes a first circuit for receiving and correlating the first signal with a set of weights and providing a correlated signal in response thereto. The weights are chosen to achieve the highest correlation with respect to the predetermined bit pattern in the transmitted signal. A second circuit is included for identifying a peak in the correlated signal and providing a bit timing output signal in response thereto. The bit timing output signal is then used by a data bit sampler for sampling data in the first signal.

5 DC OFFSET AND BIT TIMING SYSTEM AND METHOD FOR USE WITH A
WIRELESS TRANSCEIVER

INTRODUCTION

10 BACKGROUND OF THE INVENTION

The present invention relates to systems and methods for wireless data transmission. More specifically, the present invention relates to systems and methods 15 for improving DC offset and bit timing in Bluetooth-enabled wireless transceivers.

Description of the Related Art:

A wireless technology called 'Bluetooth' is under development to enable ease 20 of synchronization and mobility for a plethora of corporate and consumer applications. Bluetooth technology will open up many possibilities for quick, temporary (ad-hoc) connections with colleagues, devices, or office networks. Bluetooth is described in BLUETOOTH SPECIFICATION VERSION 1.0A CORE, published in July 1999.

25 On the receive side, Bluetooth transceivers downconvert the received signals to baseband for further processing. One processing step involves the use of correlation algorithms to improve signal-to-noise ratio (S/N). Unfortunately, certain current Bluetooth transceiver designs offer limited performance at baseband. In particular, performance limitations have been observed with respect to clock recovery 30 and direct current (DC) offset. Clock recovery refers to the process by which a received data stream is synchronized with a local clock to facilitate recovery of the transmitted data. DC offset at baseband is often caused by a frequency offset at the receiver relative to the transmitter. DC offset estimation is required to eliminate a residual DC signal resulting from the process of downconverting the received signal 35 to baseband.

Hence, a need exists in the art for a system or technique for compensating for DC offset at baseband due to frequency offsets and for improving bit timing synchronization in Bluetooth-enabled and other wireless transmission schemes.

SUMMARY OF THE INVENTION

The need in the art is addressed by the offset estimation and bit timing system and method of the present invention. The inventive offset estimation system includes a first circuit for receiving and correlating a transmitted signal and generating a 10 trigger signal in response thereto. A second circuit accumulates the received signal and provides a second signal on receipt of the trigger signal. The second signal is then converted to an offset error signal.

In an illustrative implementation, the offset estimation system is implemented in a Bluetooth-enabled wireless receiver adapted to receive a signal transmitted with a 15 known bit pattern. The received signal includes a plurality of messages, each message having at least one access code and each access code having a predetermined pattern therein for at least a portion thereof. The offset estimation system analyzes the bit pattern and detects the DC offset in the received signal.

In the illustrative embodiment, the first circuit includes an analog to digital 20 (A/D) converter having a sampling rate of N samples per bit period. The A/D converter digitizes the first signal and provides a digital input signal in response to an analog reference signal. The digital input signal is next processed to provide a correlated output signal. A peak and an edge in the correlated output signal are identified and a trigger signal is provided in response thereto. In the best mode, the 25 trigger signal is provided at a time $T = N/2$ after a time of identification of the peak.

The illustrative DC offset estimation system further includes a sliding window accumulator for providing an accumulated output signal. The accumulated output signal is latched and output on receipt of the trigger signal. Finally, the latched signal is used as an address to a lookup table which outputs and an error signal in response 30 thereto. The error signal is converted to analog and used as a reference input for the A/D converter. As an alternative, the error signal may be used to adjust the signal output by an intermediate frequency downconversion stage.

In any event, the inventive system further includes a novel arrangement for providing clock recovery and bit timing with respect to the received signal. The novel 35 bit timing system includes a first circuit for receiving and correlating the first signal with a set of weights and providing a correlated signal in response thereto. The weights are chosen to achieve the highest correlation with respect to the predetermined bit pattern in the transmitted signal. A second circuit is included for

5 identifying a peak in the correlated signal and providing a bit timing output signal in response thereto. The bit timing output signal is then used by a data bit sampler for sampling data in the first signal.

BRIEF DESCRIPTION OF THE DRAWINGS

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Fig. 1 is a block diagram of a wireless system implemented in accordance with the teachings of the present invention.

Fig. 2 is a diagram showing the format of an access code word utilized in the system of the present invention.

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Fig. 3 is a functional block diagram of an illustrative implementation of the bit timing and DC offset estimators in accordance with the teachings of the present invention.

Fig. 4 is a block diagram showing an illustrative implementation of the bit timing correlator in detail.

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Fig. 5 is a block diagram showing an illustrative implementation of the DC offset estimation correlator in detail.

Fig. 6 is a diagram illustrative of the output of the DC offset correlator utilized in the inventive system.

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Fig. 7 is a diagram showing the structure of the sliding window accumulator utilized in the inventive system.

Fig. 8 is a flow diagram of an illustrative implementation of the bit timing and DC offset methods of the present invention.

Fig. 9 is a flow diagram illustrative of the DC offset estimation method of the present invention.

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Fig. 10 is a flow diagram illustrative of the bit timing method of the present invention.

Fig. 11 shows an example of the analog baseband signal to be digitized with a DC component therein.

35

Fig. 12 is a diagram showing an optimal reference voltage level for the A/D operation.

Fig. 13 is a diagram showing the output of the A/D converter corresponding to the analog waveform depicted in Fig 12.

Fig. 14 shows a digitized waveform resulting from in incorrect reference voltage setting.

5. Fig. 15 is a diagram showing analog and digitized waveforms corresponding to "1010" pattern.

DESCRIPTION OF THE INVENTION

10. Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

15. While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

20. Fig. 1 is a block diagram of a wireless system implemented in accordance with the teachings of the present invention. In the preferred embodiment, the system 10 is a Bluetooth-enabled system. Nonetheless, those skilled in the art will appreciate that the teachings of the present invention may be utilized in other system architectures without departing from the scope thereof.

25. The system 10 includes a transmitter 20 and a receiver 30. The transmitter 20 is implemented in accordance with conventional teachings and includes first and second processing layers 22 and 24. The first processing layer 22 is a higher processing layer and includes a protocol layer and an application layer. The second processing layer 24 is a data processing layer for FEC encoding, Whiting CRC (cyclic redundancy checking) and the like. Typically, the data processing layer 24 feeds a 30. Gaussian Frequency Shift Keying filter 26 and a radio frequency (RF) modulator 28. The RF modulated signal is then transmitted via an antenna 29.

In accordance with the present teachings, the transmitter 20 transmits a signal of the form shown in Fig. 2.

35. Fig. 2 is a diagram showing the format of an access code word utilized in the system of the present invention. In accordance with the present teachings, and as discussed more fully below, the transmitter sends a code word 11 having a preamble 12 of alternating logical zeros and ones or vice versa. The preamble 11 is followed by a channel access code 14. The preamble is repeated at 16 and elsewhere throughout the code word 11 as necessary or desired for a given application. As is common in

5 the art, the access code 14 is followed by a payload header 18 and payload data 19. In accordance with the present teachings, the preamble and the access code are used to facilitate bit timing synchronization and DC offset correction in the manner discussed more fully below.

10 The transmitted signal is received by an antenna 31 of the receiver 30. The receive antenna 31 feeds a receiver front end stage 32 which is implemented in accordance with conventional teachings. That is, the front end stage 32 typically includes a downconverter, a low noise amplifier (LNA), a limiter and a discriminator. The output of the front end stage 32 is digitized by an analog-to-digital converter 34. The A/D sampling rate is N samples per bit period (N times over-sampling).

15 In accordance with the present teachings, digitized received data samples from the A/D converter 34 are provided to a bit timing estimator 36, a DC offset estimator 38 and a data sampler 40. As discussed more fully below, the bit timing estimator 36 is driven by a processor 42.

20 As per the transmission scheme, the output of the data bit sampler 40 is processed by a data processing layer 44 and a higher layer processing stage 46. As per conventional teachings, the data processing layer 44 performs FEC decoding, De-Whiting, and CRC decoding. The higher layer processing 46 performs protocol layer and application layer processing in a conventional manner.

25 As mentioned above, a DC offset is caused by a frequency offset between the transmitter 20 and the receiver 30 in combination with any DC components added along the receive path. The DC offset effect seen at the baseband receiver input is actually the DC component of the analog signal relative to the reference voltage of the A/D converter. In other words, if the A/D converter reference voltage equals the DC component of the analog waveform, the DC offset seen at the A/D output will be 30 zero. Therefore, the purpose of the DC offset estimation module is to estimate the DC offset from the digital signal. According to the present teachings and as discussed more fully below, the preamble is used to estimate DC offset at the receiver. The estimate is then used to tune the receiver by either adjusting the reference voltage for the A/D 34 or, alternatively, at the front end 32 through an AFC (automatic frequency 35 control) signal.

Further, in accordance with the present teachings and as discussed more fully below, bit timing is optimized by analyzing the received signal for a correlation between the received signal and a correlation template. The correlate template can be

5 the full channel access code or a portion of the channel access code. The correlation peak yields the optimal sampling time for the data bits in the payload portion 19 of the received signal. Hence, particularly novel aspects of the present invention are the bit timing and the DC offset estimators 36 and 38, respectively.

10 Fig. 3 is a functional block diagram of an illustrative implementation of the bit timing and DC offset estimators in accordance with the teachings of the present invention. The bit timing estimation subsystem 36 consists of a first (bit timing) correlator 50 and a peak detector 52.

15 The A/D converter 34 provides input to the bit timing correlator 50 in the bit timing estimator 36. The A/D converter 34 also provides input to a second (DC offset) correlator 54 (correlator 2) and a sliding window accumulator 56 disposed in the DC offset estimation subsystem 38. As discussed more fully below, the first correlator 50 searches the digitized data stream for the presence of the channel access code 14 in each code word 11 sent by the transmitter 20 and received by the receiver 30. The second correlator 54 examines the digitized data stream for the presence of 20 the preamble 12 in each code word 11 (i.e., in the illustrative embodiment, a "1010" pattern).

25 Fig. 4 is a block diagram showing an illustrative implementation of the bit timing correlator in detail. In the illustrative embodiment, the bit timing correlator 50 is implemented with $N \times (M-1) + 1$ shift registers 51 - 63 (odd numbers only) connected in a cascade arrangement, where N is the sampling rate of the A/D converter 34 as mentioned above. The shift registers 51 - 63 store incoming data samples from the A/D converter 34. For the case of a baseband A/D conversion with only one bit resolution, each shift register is implemented with a flip-flop.

30 The data samples stored in the shift registers are correlated with coefficients c_1, c_2 through c_M via a multiplication operation implemented with exclusive-NOR (XNOR) gates (65, 69, 73 and etc.), respectively, where the correlation pattern is C_j , $j=1, 2, \dots, M$. The correlator coefficients (C_j) are stored in shift registers 67, 71, ..., 75 and etc. The correlator 50 matches M bits from the access code pattern where, in the illustrative embodiment, $M = 1, 2, \dots, 64$. Those skilled in the art will appreciate 35 that the illustrative implementation of the bit timing correlator 50 allows for the template (or the bit pattern for correlation) to be configurable and downloadable based on a desired access code.

5 As discussed more fully below, the next step in the correlation involves a summation operation using a counter 77. The counter 77 counts the number of 1s at the output of the exclusive-NOR gates. When the input binary samples entering the exclusive-NOR gates 65, 69, 73 and etc., correlate with the access code stored in the shift registers 67, 71 . . . 75 and etc., respectively, the output of the counter 77 will be
10 at a peak. The peak timing identifier 52 then processes the output of the bit timing correlator 50 to find this peak in the correlated data values.

The peak is identified by comparing the correlated values result against a threshold using a conventional peak detector. When a peak is detected, the peak location provides an initial sampling time for bit timing. The output of the bit timing
15 correlator 50 has the same sampling rate as the A/D sampling rate. Accordingly, the subsequent data bits can be optimally sampled at every N samples after the peak location. This optimal sampling time will not change for the duration of the packet.

It should be noted that depending on the length M of correlator 50, the peak location may not be at the end of the access code. For example, if the length M=64,
20 the peak location will be the end of the access code and the first bit in the packet header can be sampled at the fifth bit time slot after the peak location (to skip over the preamble "1010" or "0101" tail bits). If M is less than 64, then a sequence of 64-M+4 bits have to be skipped to go to the packet header field.

25 Returning to Fig. 3, in the illustrative embodiment, the DC offset estimation subsystem 38 includes a second (DC offset) correlator 54, a second peak timing identifier 58, a latch 60, a sliding window accumulator 56, and a reference voltage level converter 62.

30 Fig. 5 is a block diagram showing an illustrative implementation of the DC offset estimation correlator in detail. The illustrative implementation of the DC offset estimation correlator 54 is similar to that of the bit timing correlator 50. That is, the DC offset correlator 54 includes Nx3+1 shift registers 81 - 99 (odd numbers only) connected in cascade to store the incoming digitized data samples. The coefficients
35 c_0, c_1, c_2 and c_3 shown in Fig. 5 and used in the illustrative embodiment for DC offset estimation are $c_0=0, c_1=1, c_2=0, c_3=1$. For the case of a baseband A/D converter 34 with only one bit resolution, each shift register is implemented using a flip-flop, the multiplication is implemented using exclusive-NOR gates 101 - 107 (odd numbers only) and the summation is implemented using a counter 109. The counter 109 counts number of 1s at the output of a set of four exclusive-NOR gates 101 - 107 (odd

5 numbers only). When the input binary samples entering the four exclusive-NOR gates are equal to the preamble 12 in the code word 11 (i.e., 1010) the counter output will be at its peak with a value of 4.

10 Fig. 6 is a diagram illustrative of the output of the DC offset correlator 54. The output of the DC offset correlator 54 is a time domain sequence having the same rate as the A/D sampling rate. The output of the DC offset correlator 54 is input to a peak timing identifier and edge detector 58.

15 The peak timing identifier and edge detector 58 detects the peak location and calculates the time T (shown in Fig. 6) at N/2 samples after the peak location. The trigger signal generated by the peak timing identifier and edge detector 58 will be at the timing T (shown in Fig. 6), which is N/2 samples after the peak timing. This function can be implemented either in software running on a processor, with gates in a 20 FPGA (field programmable gate array) or in an ASIC (application specific integrated circuit). A threshold should be used to qualify the peak; that is, the peak has to be higher than a threshold to be considered as a peak. Practically, since only the 4-bit preamble 12 (the 1010 pattern) is used for correlation (the correlator 54), the threshold should be set to be 4. Thereafter, the candidate values are compared to identify the peak. On detection of the peak, a trigger signal will be generated by the peak timing identifier and edge detector 58.

25 As shown in Fig. 3, the trigger signal is received by a latch 60 and used to latch the output of the sliding window accumulator 56. In the preferred embodiment, the trigger signal is generated at time T shown in Figure 6.

30 The structure of the sliding window accumulator is shown in Fig. 7. The accumulator 56 is similar to the correlators 50 and 54 in construction with the exception that it does not employ the use of XNOR gates. That is, the accumulator 56 includes a plurality of shift registers 111 - 125 arranged in a cascade form which feed a summer 127. For the illustrative case of an analog to digital converter 34 having one bit resolution, the shift registers 111 - 125 are implemented with flip-flops and the summation is implemented using a counter. When the DC offset correlator 54 and peak timing identifier 58 find the preamble, the value stored in the sliding window accumulator 56 is latched for output. As illustrated in Fig. 7, the width of the window used by the sliding window accumulator is set by the number of shift registers, which is a period of 4 bits.

5 Returning to Fig. 3, if the bit pattern is "1010" and sampling rate is 4 times over-sampling, an output value of 8 from the latched 60 corresponds to no DC offset. A smaller value indicates the reference voltage is higher than the DC component of the analog signal and a value higher than 8 indicates that the reference voltage is too low relative to the DC component of the analog signal.

10 In any event, the latched accumulator output is converted to a proper control signal by a reference voltage level converter 62. The reference voltage level converter 62 may be implemented with a lookup table. On receipt of the output of the sliding window accumulator, the converter 62 looks up an appropriately scaled voltage to be fed back to the A/D converter 34 via a digital-to-analog converter 64 as 15 a reference voltage to control the DC offset seen in the digital domain.

As mentioned above, as an alternative, a signal can be generated converter 62 for AFC feedback control, based on the estimated DC offset, to adjust the frequency of the IF stage in the receiver front end 32 illustrated in Fig. 1. This approach involves a change in the DC component of the analog signal to match the reference 20 voltage for the A/D converter.

A processor 42 receives input via an interface 43 and provides weights for the first and second correlators 50 and 54 allow for system reconfiguration.

The method of operation of the inventive system is illustrated in Figs. 8 - 10.

Fig. 8 is a flow diagram of an illustrative implementation of the bit timing and 25 DC offset methods of the present invention. As illustrated in Fig. 8, the method 200 includes the step 202 of receiving the transmitted signal, storing samples in a buffer and incrementing a time counter modulo N. At step 204, the system checks for data mode. If data mode is not set, at step 300, the system performs DC offset estimation and correction.

Fig. 9 is a flow diagram illustrative of the DC offset estimation method of the 30 present invention. At step 304 correlator 2 (Fig. 3) processes the signal looking for the preamble 12. At step 306, the output of the correlator is processed for peak detection by the peak timing identifier 58 of Fig. 3. If the peak is detected, at step 308, the system checks for a zero crossing at the end of the preamble at step 310. Next, at step 312, the DC value is calculated at step 312. As is well known in the art, 35 the DC value is calculated by averaging the sample values. At step 314, the new DC estimated value is averaged with the DC offset estimate history by the processor 42. This is achieved by adding the accumulator output to an accumulated sum each time

5 when it is latched and then divide the accumulated sum by the number of times the 1010 bit pattern is detected during the channel access code period. At step 316, the averaged value is converted to a reference voltage by the converter 62 and at step 318, output as a reference voltage for the A/D converter 34 of an AFC control voltage for the RF front end 32.

10 Returning to Fig. 8, at step 400, bit timing estimation is next performed. Fig. 10 is a flow diagram illustrative of the bit timing method of the present invention. At step 404, correlator 1 processes the received data samples and performs full or partial channel access code pattern correlation. At step 406, the peak timing identifier 52 (Fig. 3) looks for a peak in the correlation. On the detection of a peak, at step 410, the system sets current sampling time as data mode demodulation sampling time and the data mode flag will be set. The sampling time refers to the timing of the sample to be used for each bit duration. More specifically, if the number of samples per bit is N, then the bit timing correlator (correlator 1 50) peak timing marks the timing that every N samples after the peak will be used as the bit sampled for each bit period. Note 15 that, the correlation output yields by the correlator 1 50 at the peak may show a flat level for several sampling times. If this happens, the mid-point sample timing of the flat period will be chosen to be the true peak timing. If the peak is not detected at step 408, the data mode remains "no".

20 Returning to Fig. 8, when, at step 204 the data mode is found to be "yes", then 25 at step 210, the system processes the received data. In Fig. 1, data output by the A/D converter is sampled by a bit sampler 40 with timing provided by the bit timing estimator 36. The output of the bit sampler 40 is processed by a receiver data processor 44. As mentioned above, the receiver data processor 44 performs FEC decoding, De-Whiting, and CRC checking. Next, the higher layer processor 46 30 performs protocol and application layer processing until the end of the received signal processing at step 216 in Fig. 8.

DC OFFSET ESTIMATION

Fig. 11 shows an example of the received analog baseband signal with a DC component therein to be digitized at the baseband receiver using the A/D 34. The AC component of the waveform in Fig. 11 is the result of 1 and 0 digital patterns generated by the transmitter 20 passing through the GFSK filter 26 before the RF modulator 28. Again, for the illustrative embodiment, the A/D 34 is assumed to have only one-bit resolution. Those skilled in the art will appreciate that the present teachings can be directly applied to an A/D with N-bit resolution without departing from the scope thereof. Ideally, the system will adjust the A/D reference voltage to be equal to the DC level of the analog input signal. This is depicted in Fig. 12 below.

Fig. 12 is a diagram showing an optimal reference voltage level for the A/D operation. In this case, the reference voltage equals the DC component of the analog signal.

Fig. 13 is a diagram showing the output of the A/D converter corresponding to the analog waveform depicted in Fig 12. Note that, 4 times over-sampling is used as an exemplary A/D sampling rate for the illustrative embodiment. (Those skilled in the art will appreciate that the present teachings are not limited to any particular sampling rate.) The digitized output shows equally distributed 1s and 0s.

If the reference voltage of the A/D is not set to be the DC component of the analog signal, the result of the A/D output will be biased as shown in Fig 14.

Fig. 14 shows a digitized waveform resulting from an incorrect reference voltage setting. Fig. 14 shows the resulting asymmetrical distribution of 1s and 0s.

As discussed above, the DC estimation system and method of the present invention searches for a pre-determined bit pattern, i.e., the preamble 12, and uses this pattern for DC offset estimation. The bit pattern should be a certain pattern where DC offset can be estimated from the digital RX signal generated by that pattern. The illustrative pattern "1010" is such a pattern that can be used for DC offset estimation.

Fig. 15 is a diagram showing analog and digitized waveforms corresponding to "1010" pattern. In Fig. 15, it is assumed that the DC offset at the digital output is zero. Correlator 2 identifies the "1010" patterns in the manner discussed above. When the pattern is identified, a trigger signal is generated that latches the sliding window accumulator output value. The sliding window accumulator accumulates the

5 same period of signals corresponding to "1010" bit patterns. For the case of 4 times over-sampling rate, the sliding window accumulator adds the most current 16 samples if "1010" is the pattern for DC offset estimation.

10 The trigger will be generated at time T shown in Figure 6. If the "1010" pattern in Figure 15 is considered, the time trigger occurs exactly at the moment where the output of the accumulator is the sum of the 16 digital samples shown in Figure 15.

15 If the bit pattern is "1010" and sampling rate is 4 times over-sampling, an output value of 8 from the latched counter output corresponds to no DC offset. A smaller value indicates the reference voltage is higher than the DC component of the analog signal, and a value bigger than 8 indicates the reference voltage is too low relative to the DC component of the analog signal.

As discussed above, the latched accumulator output is converted to a proper control signal for feeding back to the analog circuit to control the DC offset seen at the digital waveform.

20 The DC offset estimation unit should be activated as soon as the system (e.g., Bluetooth) slot-processing window begins. It should remain active during the access code portion or it can be active for the entire packet receiving period. During its active period, it continuously searches for the pre-determined bit pattern and adjusts the analog circuit whenever the bit pattern is detected. If multiple bit patterns are 25 detected, the estimated DC offset from different patterns should be averaged to give a better DC offset estimation.

Bit Timing Estimation

30 As mentioned above, in Fig. 3, correlator 1 matches M bits from the access code pattern where $M=1, 2 \dots 64$. The peak timing identifier 52 will process the output of correlator 1 to find the peak. The output of the correlator 1 has the same sampling rate as the A/D sampling rate. The peak will be checked against a threshold. Once a peak is detected, the peak location is exactly the best sampling time for bit 35 slicing. The rest of the data bits can be sampled at every N samples after the peak location. The best sampling time will not be changed for the entire packet duration.

Depending on the length M of correlator 1, the peak location may not be the end of the access code. For example, if the length $M=64$, the peak location will be the

5 end of the access code and the first bit in the packet header can be sampled at the fifth bit timing after the peak location (to skip over the "1010" or "0101" tail bits). If M is less than 64, $64-M+4$ bits has to be skipped to go to the packet header field.

10 Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

15 Accordingly,

WHAT IS CLAIMED IS:

CLAIMS

1. A system for estimating an offset in a signal comprising:
 - first means for receiving and correlating a first signal and generating a trigger signal in response thereto;
 - 10 second means for accumulating said first signal and providing a second signal on receipt of said trigger signal; and
 - third means for converting said second signal to an offset error signal.
2. The invention of Claim 1 further including a wireless transmitter adapted to transmit said first signal with a predetermined bit pattern therein for a least a portion thereof.
- 15 3. The invention of Claim 2 wherein said pattern consists of alternating logical '0' and logical '1' bits for at least a portion thereof.
- 20 4. The invention of Claim 3 wherein said first signal includes a plurality of messages, each message having at least one access code and each access code having said pattern therein for at least a portion thereof.
- 25 5. The invention of Claim 1 wherein said first means includes means for digitizing said first signal to provide a digital input signal in response to an analog reference signal and a correlator for correlating said digital input signal to provide a correlated output signal.
- 30 6. The invention of Claim 5 wherein said first means further includes means for identifying a peak in said correlated output signal and providing said trigger signal in response thereto.
- 35 7. The invention of Claim 6 wherein said first means further includes means for finding an edge in said correlated output signal and providing said trigger signal in response thereto.
8. The invention of Claim 7 wherein said trigger signal is provided at a time $T = N/2$ after a time of identification of said peak.

5 9. The invention of Claim 5 further including means for providing bit timing.

10. 10. The invention of Claim 9 wherein said means for providing bit timing includes means for correlating the output of said means for digitizing said first signal to provide a correlated signal.

11. 11. The invention of Claim 10 wherein said means for providing bit timing further includes means for identifying a peak in said correlated signal to provide a bit timing output signal.

15 12. The invention of Claim 1 wherein said second means includes a sliding window accumulator for providing an accumulated output signal.

20 13. The invention of Claim 1 wherein said third means includes means for comparing said second signal to a reference signal and generating error signal in response thereto.

25 14. A wireless receiver adapted to estimate a direct current offset in a received signal, said system having a wireless transmitter adapted to transmit said first signal with a predetermined bit pattern therein for at least a portion thereof, said receiver comprising:

first means for receiving and correlating a first signal and generating a trigger signal in response thereto, said first means including:

30 an analog to digital converter having a sampling rate of N samples per bit period for digitizing said first signal to provide a digital input signal in response to an analog reference signal and

means for correlating said digital input signal to provide a correlated output signal, said means for correlating further including means for identifying a peak in said correlated output signal and means for finding an edge in said correlated output signal and providing said trigger signal at a time $T = N/2$ after a time of identification of said peak in response thereto;

35 second means for accumulating said first signal and providing a second signal on receipt of said trigger signal, said second means including a sliding window accumulator; and

5 third means for converting said second signal to an offset error signal, said third means further including means for converting said error signal to said analog reference signal.

10 15. The invention of Claim 14 wherein said first signal includes a plurality of messages, each message having at least one access code and each access code having said pattern therein for at least a portion thereof.

15 16. The invention of Claim 14 wherein said third means includes means for comparing said second signal to a reference signal and generating error signal in response thereto.

17. The invention of Claim 14 further including means for correlating the output of said means for digitizing said first signal to provide a correlated signal.

20 18. The invention of Claim 17 wherein said means for providing bit timing further includes means for identifying a peak in said correlated signal to provide a bit timing output signal.

25 19. A system comprising:
first means for receiving and correlating a first signal with a predetermined signal and providing a correlated signal in response thereto and
second means for identifying a peak in said correlated signal and providing a bit timing output signal in response thereto.

30 20. The invention of Claim 19 wherein said system includes a data bit sampler for sampling data in said first signal in response to said bit timing output signal.

35 21. The invention of Claim 20 further including a wireless transmitter adapted to transmit said first signal with a predetermined bit pattern therein for a least a portion thereof.

40 22. The invention of Claim 21 wherein said first signal includes a plurality of messages, each message having at least one access code and each access code having said pattern therein for at least a portion thereof.

5

23. The invention of Claim 22 wherein said system further includes a wireless receiver adapted to receive said first signal.

24. A method for estimating an offset in a signal including the steps of:
10 receiving and correlating a first signal and generating a trigger signal in response thereto;
accumulating said first signal and providing a second signal on receipt of said trigger signal; and
converting said second signal to an offset error signal.

15

25. A method for bit timing including the steps of:
receiving and correlating a first signal with a predetermined signal and providing a correlated signal in response thereto and
identifying a peak in said correlated signal and providing a bit timing output signal in
20 response thereto.

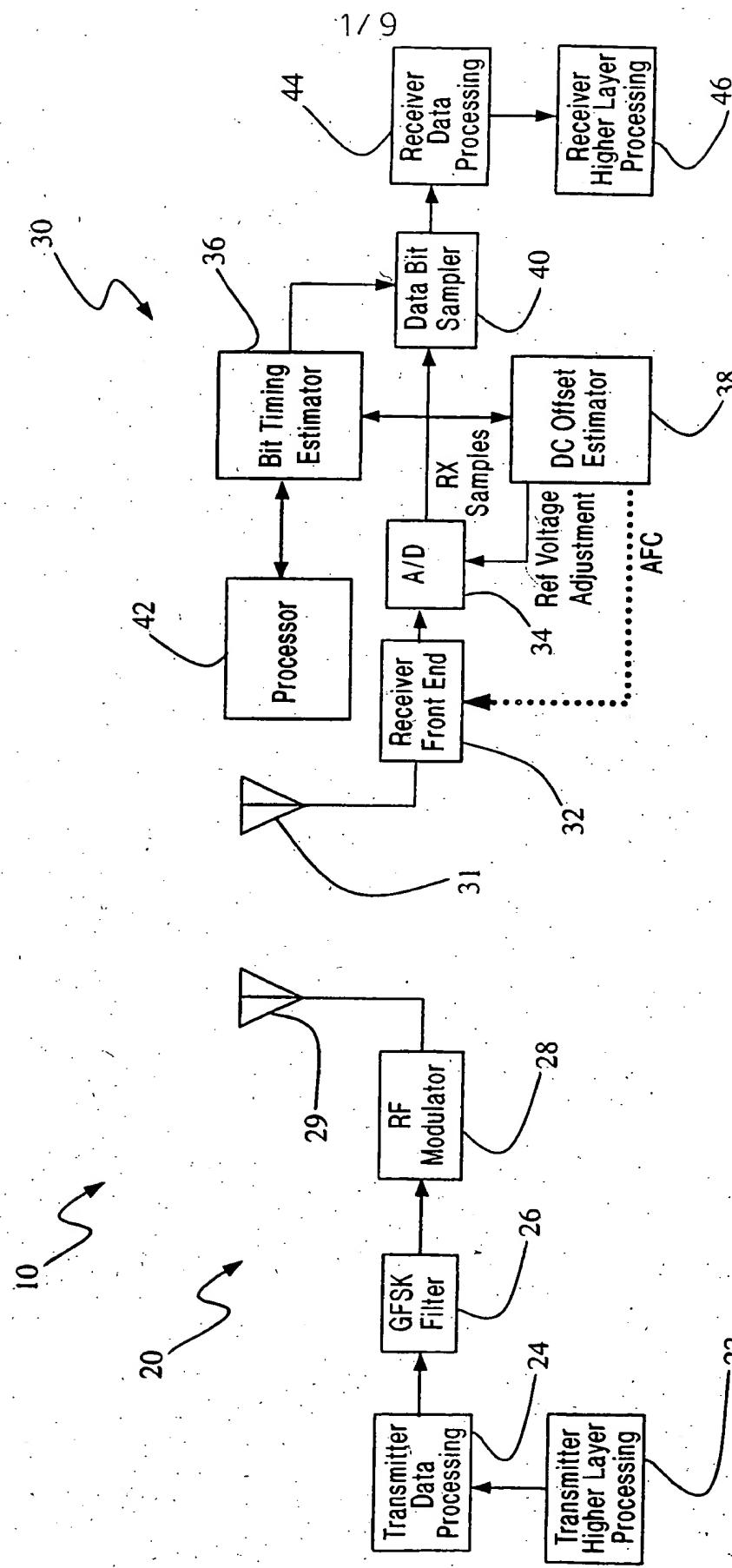


FIG. 1

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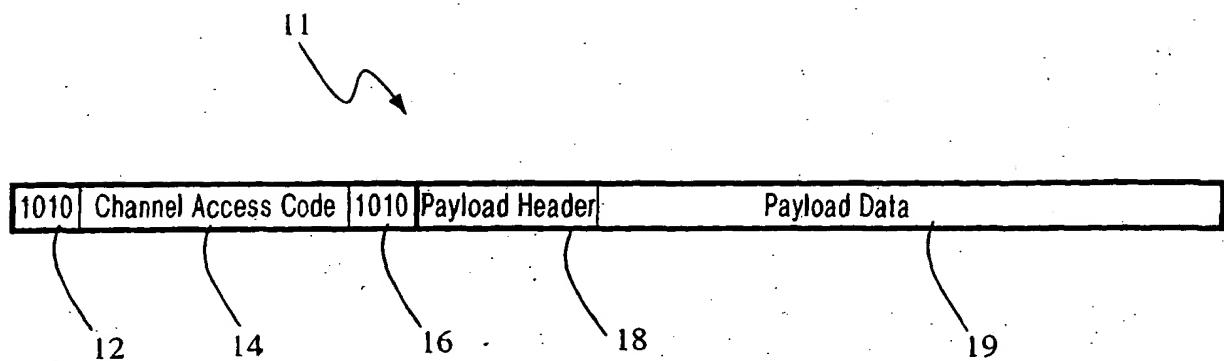


FIG. 2

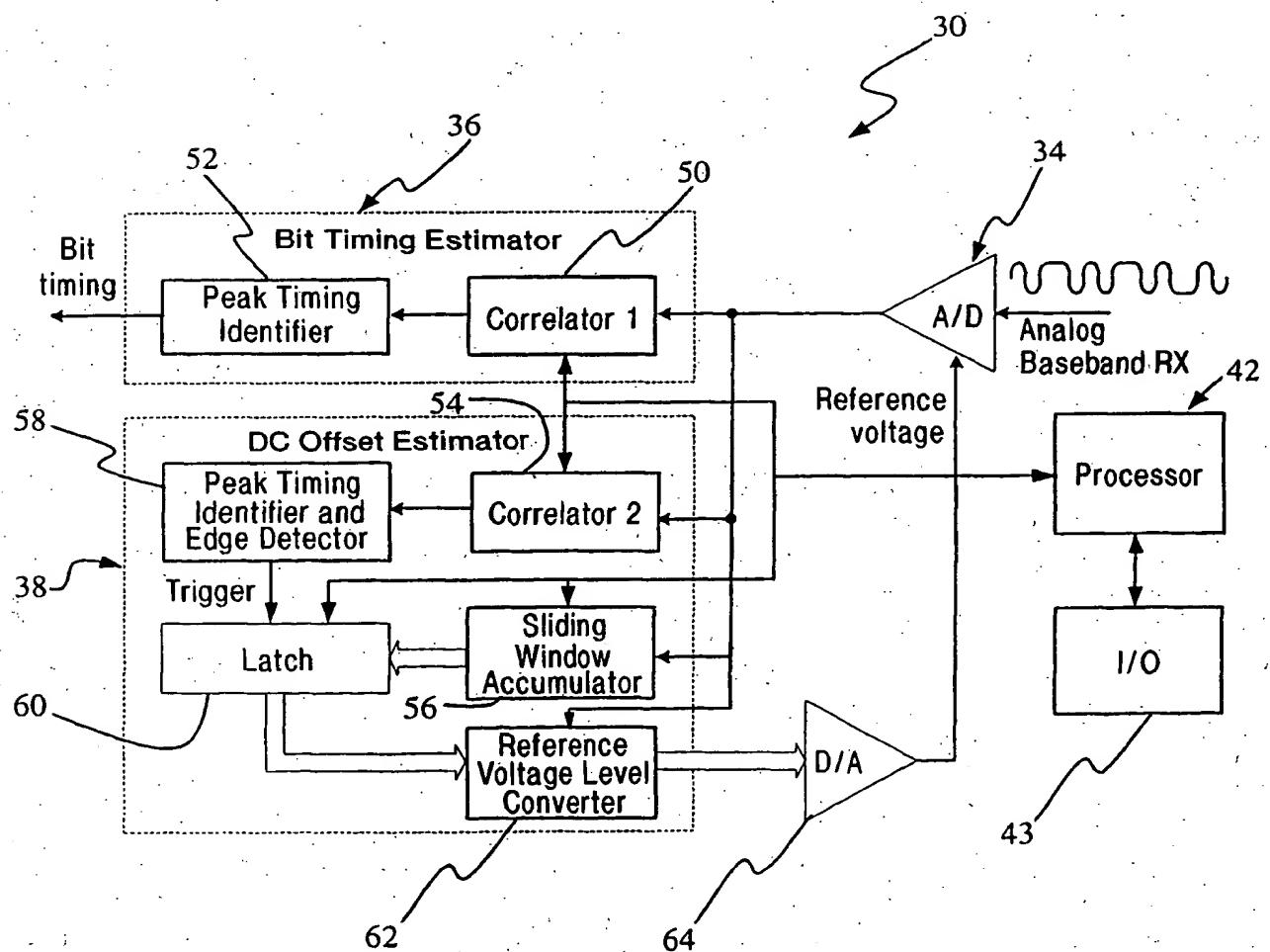


FIG. 3

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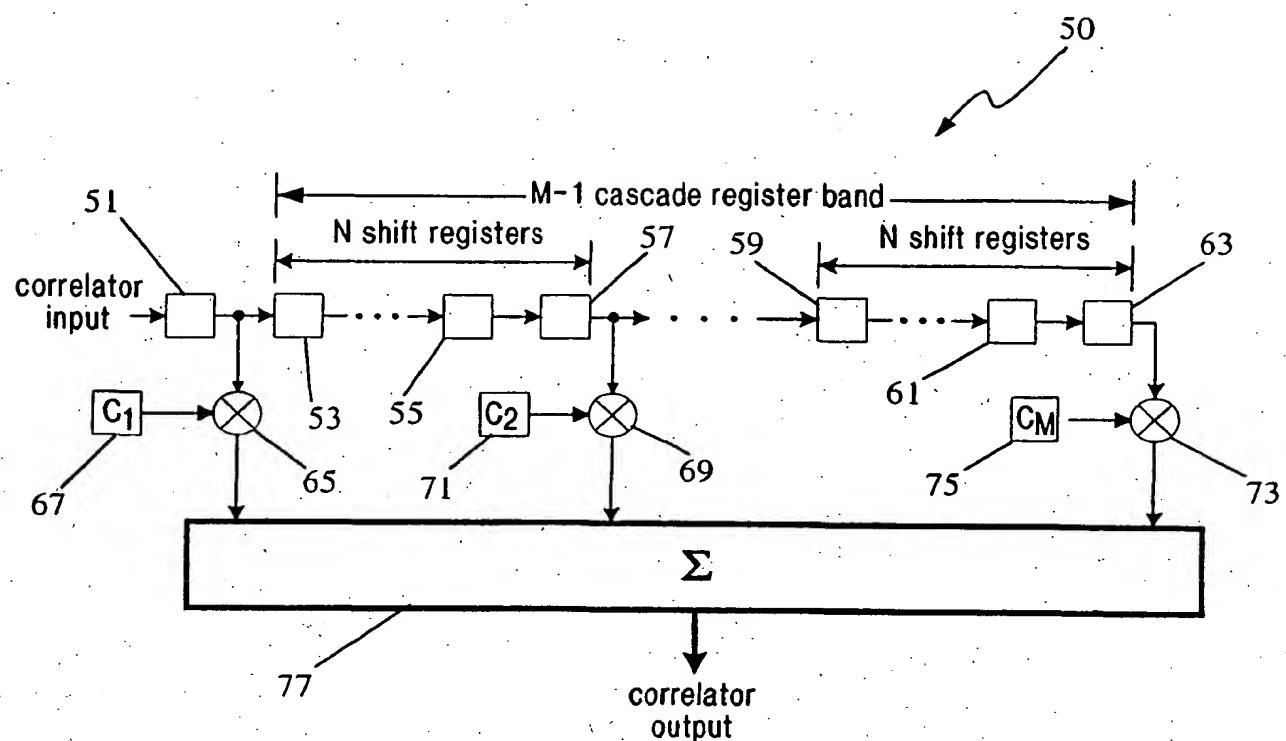


FIG. 4

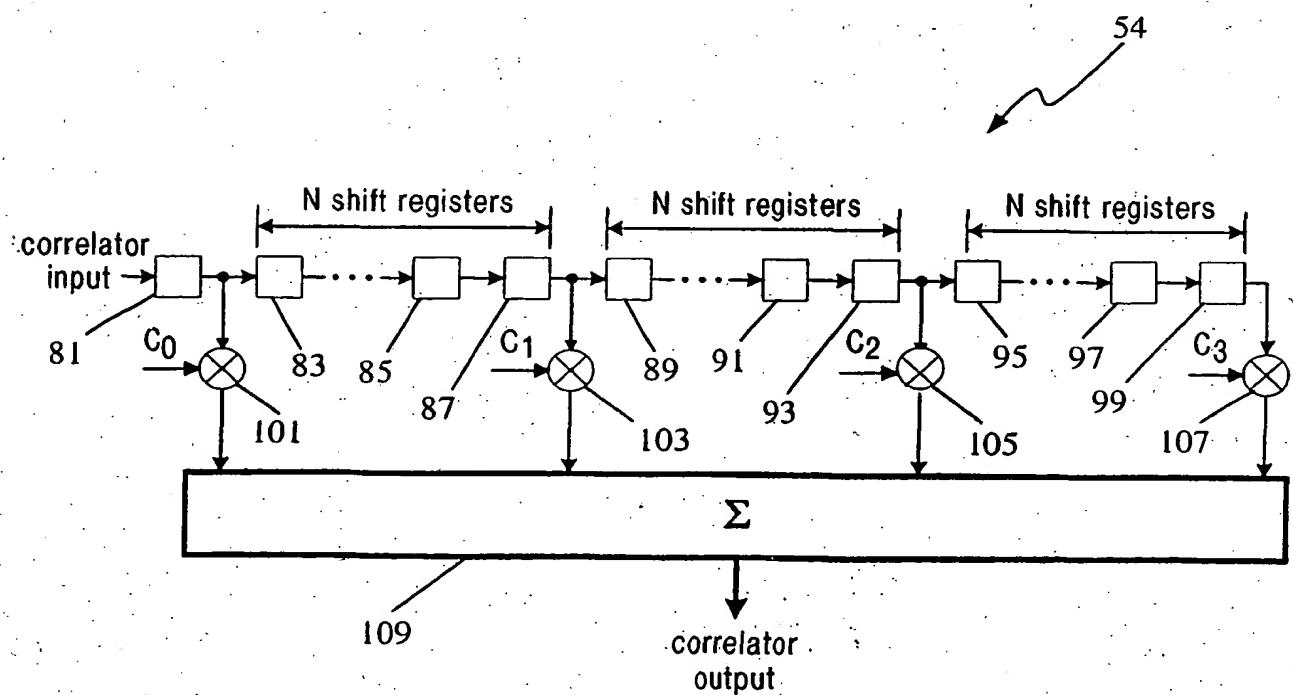


FIG. 5

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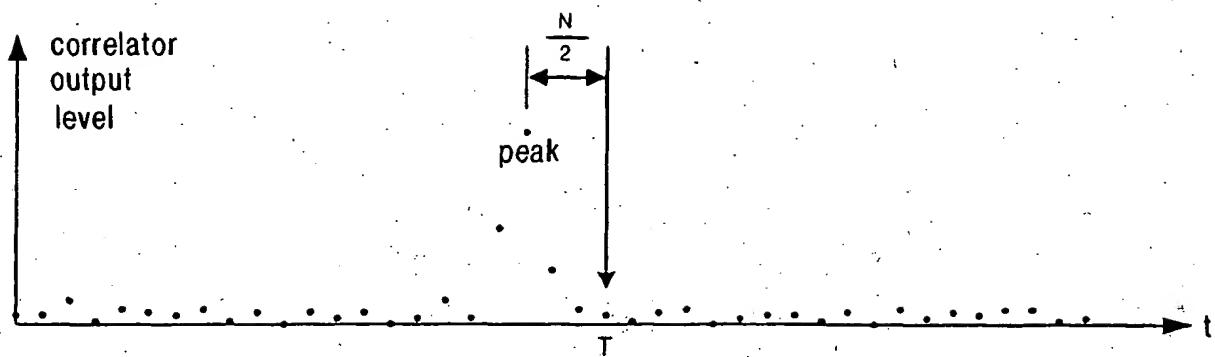


FIG. 6

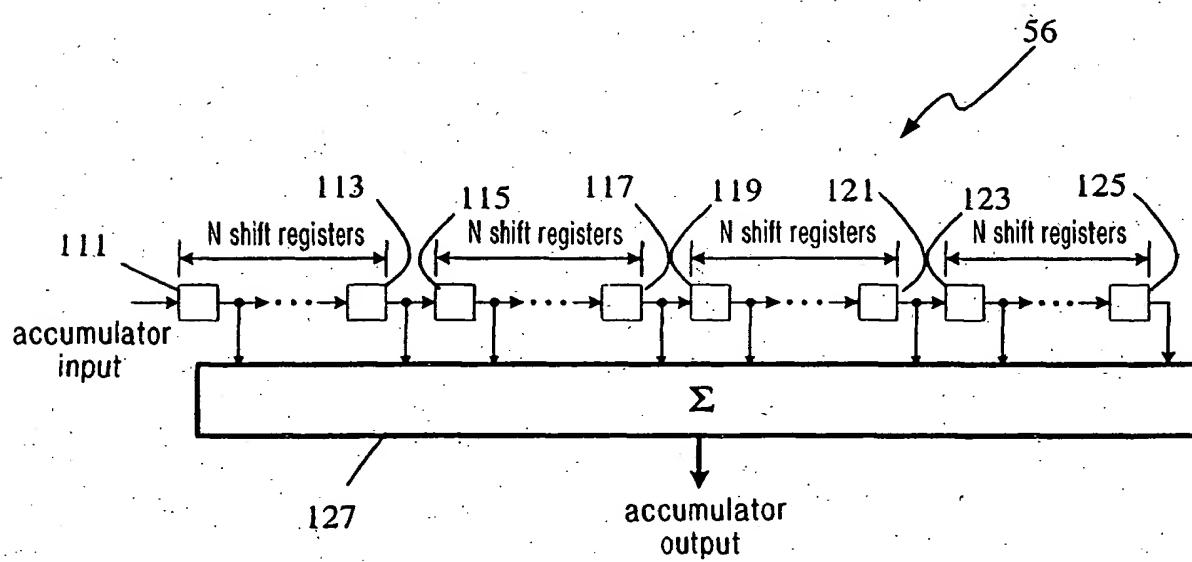


FIG. 7

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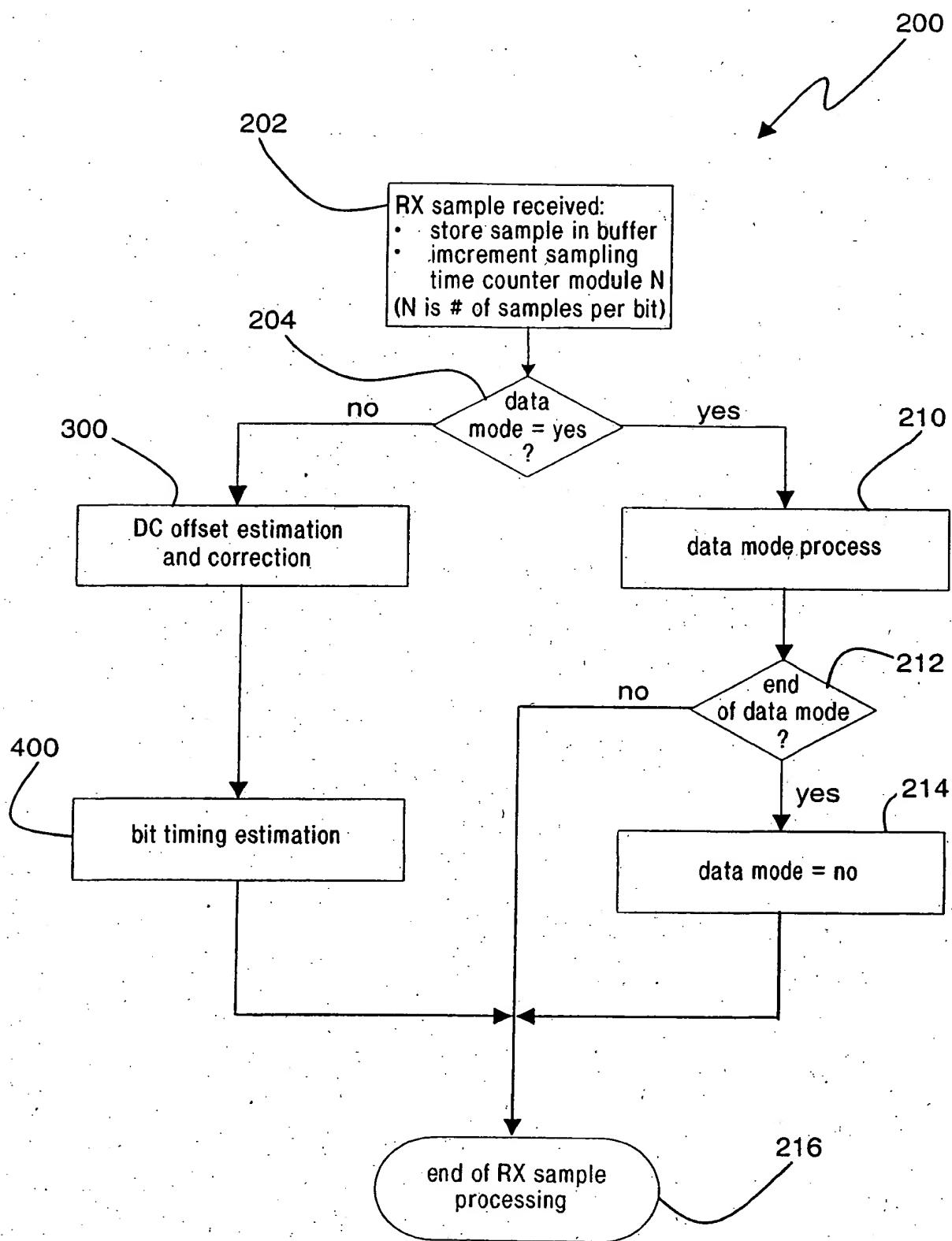


FIG. 8

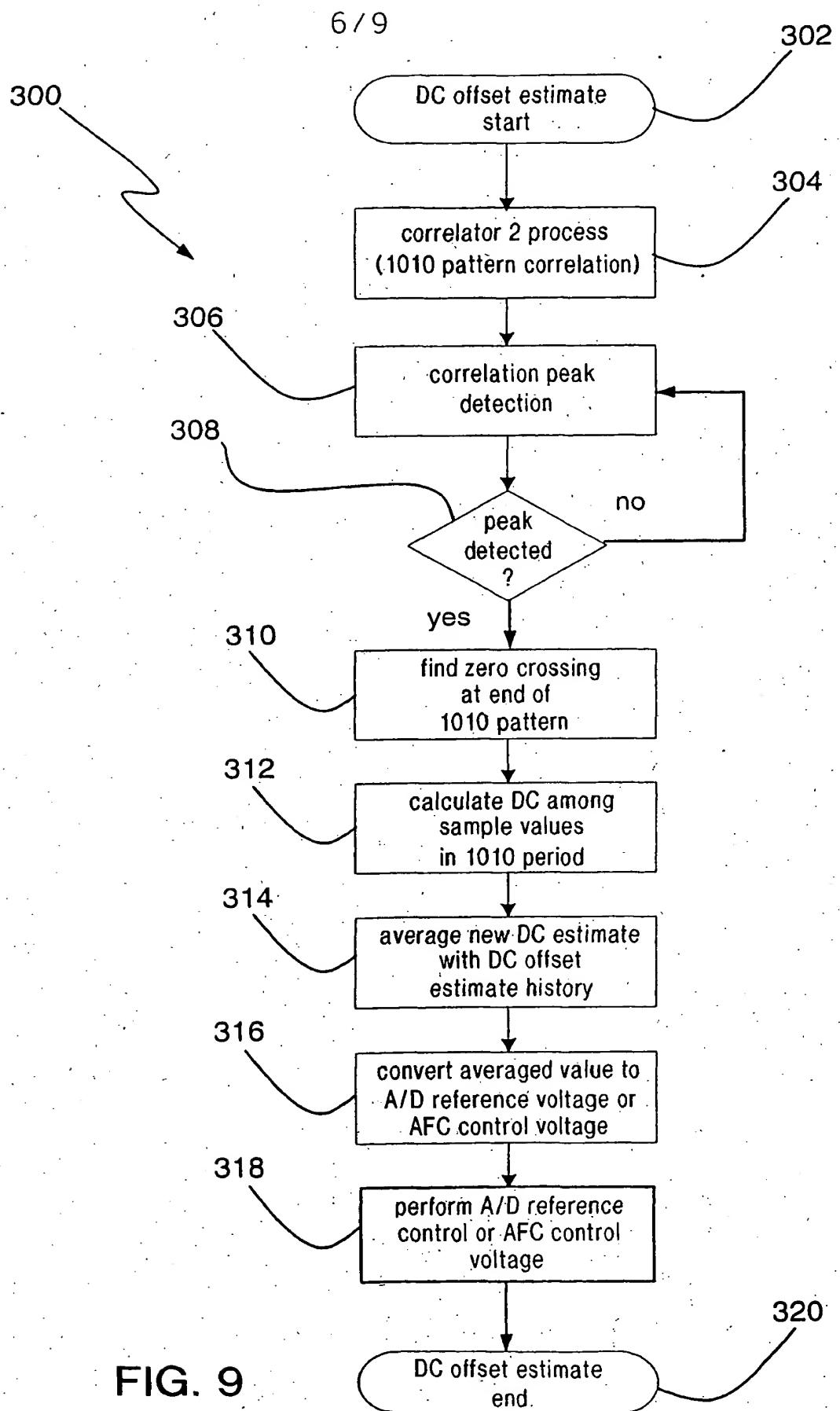


FIG. 9

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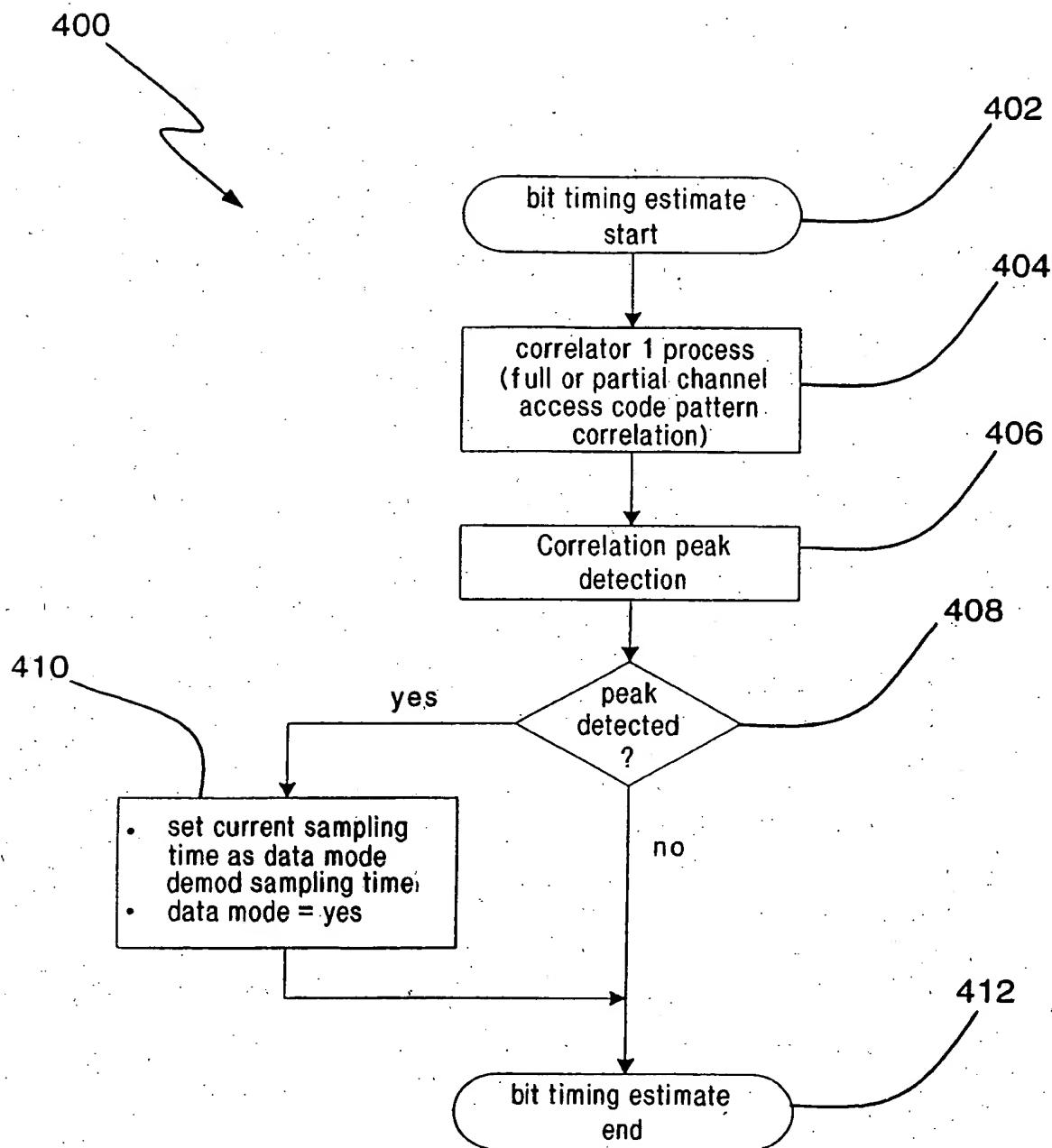


FIG. 10

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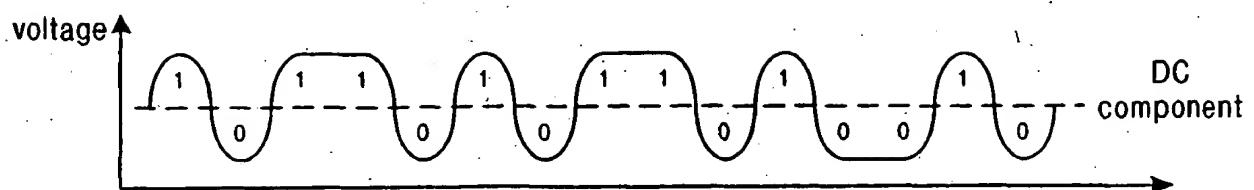


FIG. 11

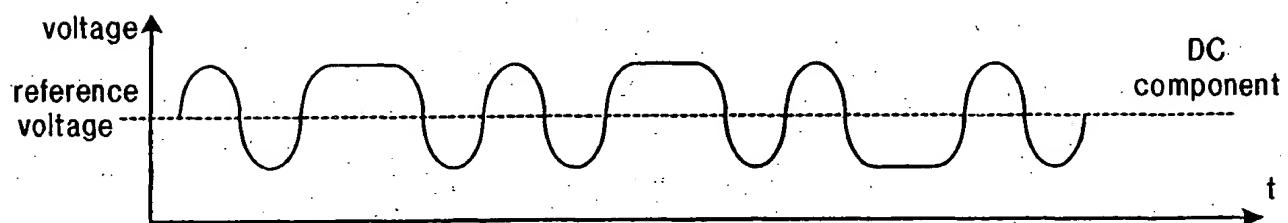


FIG. 12

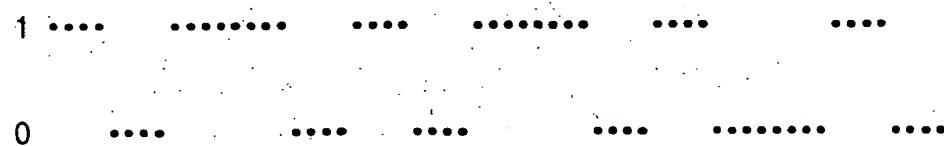


FIG. 13

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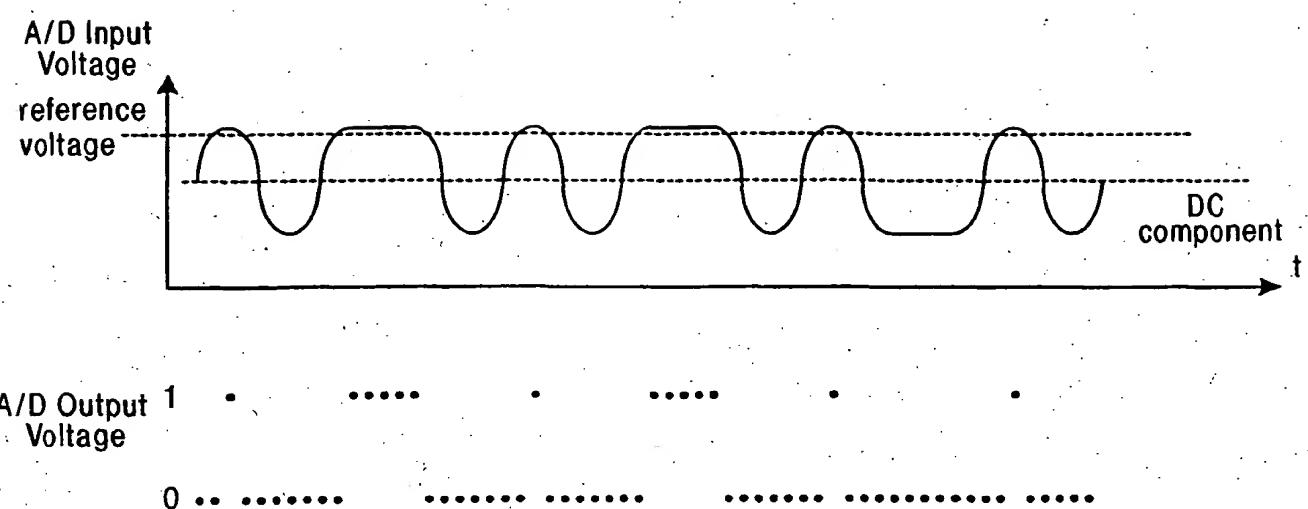


FIG. 14

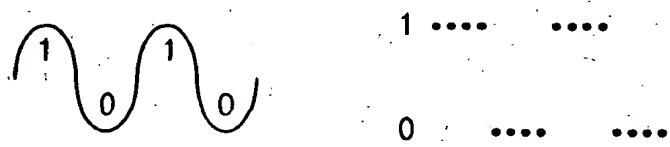


FIG. 15